

REMARKS

The present amendment is in response to the *Advisory Action* dated April 15, 2003. By the present amendment, claims 18 and 58 have been amended. Accordingly, claims 18-33 and 58-66 are pending in the application. In light of the accompanying Request for Continued Examination filed under 37 CFR §1.114, the above amendments, and the following remarks, reconsideration and allowance of pending claims 18-33 and 58-66 are respectfully requested.

A. Objection to drawings under 37 CFR §1.83(a)

In the *final rejection* dated October 21, 2002, the Examiner had objected to the drawings under 37 CFR §1.83(a) for failing to show every feature of the invention specified in the claims. Specifically, the Examiner has requested that the drawings show the electrical connection between the thermally conductive vias and the heat spreader. Applicant respectfully traverses the objection for the reasons that follow. With reference to Figure 2 and page 5, lines 20-28, of present application, heat spreader 290 is shown on lower surface 210 of substrate 220 and is directly connected to first group of vias 255. With this arrangement, first group of vias 255 provide electrical and thermal pathways from upper surface 200 to lower surface 210 and to heat spreader 290 which is directly attached to lower surface 210 and to first group of vias 255. Likewise, with reference to Figure 5, heat spreader 290 is also shown on lower surface 210 of substrate 220 and is directly connected to first group of vias 255 for thermal and electrical conductivity.

Accordingly, applicant respectfully submits that the drawings show the electrical connection between the thermally conductive vias and the heat spreader, and that, therefore, the objections to the drawings should now be withdrawn.

B. Rejection of claim 61 under 35 USC §112, Second Paragraph

In the *final rejection* dated October 21, 2002, the Examiner had rejected claim 61 under 35 USC §112, Second Paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Specifically, the Examiner has requested clarification on how the heat spreader is electrically connected to the thermally conductive vias. As discussed above, Figures 2 and 5 illustrate the direct connection between first group of vias 255 and heat spreader 290 for electrical and thermal connectivity. With reference to Figure 2, heat spreader 290 is shown on lower surface 210 of substrate 220 and is directly connected to first group of vias 255. With this arrangement, first group of vias 255 provide electrical and thermal pathways from upper surface 200 to lower surface 210 and to heat spreader 290 which is directly attached to lower surface 210 and to first group of vias 255. For the foregoing reasons, applicant respectfully submits that the rejection of claim 61 under 35 USC §112, Second Paragraph, has been traversed and that, therefore, claim 61 should now be allowed.

C. Rejection of claims 18-20, 22-33 and 58-66 Under 35 USC §102(b)

In the *final rejection* dated October 21, 2002, the Examiner had rejected claims 18-20, 22-33 and 58-66 under 35 USC §102(b) as being anticipated by Selna (USPN 5,640,048) ("Selna '048"). Applicant respectfully disagrees; however, in order to expedite the prosecution of this application, applicant has amended independent claims 18 and 58 to further specify that the heat spreader is "directly attached" to the bottom surface of the substrate. For the reasons that follow, applicant respectfully submits that independent claims 18 and 58 are patentably distinguishable over Selna '048.

Selna '048 discloses ball grid array (BGA) package 50 which can be interfaced to PCB 18. Selna '048, however, fails to disclose or suggest providing a heat spreader directly attached to bottom surface of the substrate of BGA package 50 as specified in claims 18 and 58. In the present Office Action, the Examiner references package trace 10C on the bottom surface of BGA package 50 of Selna '048 as disclosing a heat spreader. However, package trace 10C is not a heat spreader, but rather is an electrical trace between vias 6C and BGA traces 14C. Instead, Selna '048 positions a heat spreader (Vss plane 20C) on PCB 18, rather than positioning the heat spreader directly attached to the bottom surface of BGA package 50 (see, e.g., Figure 2 and 3, Col. 6:50-56). This arrangement in Selna '048 wherein the heat spreader is positioned on the PCB, and, thus, is not directly attached to the bottom surface of BGA package 50, is acknowledged by the

Examiner on Page 4 of Detailed Action. Moreover, the substrate in Selna '048 would not support a large heat spreader directly attached to the bottom surface of BGA package 50, because, such an arrangement would interfere with the proper positioning of ball grids 14c, relative to ball grids 10a and 10b, and would thus render BGA package 50 unsuitable for interfacing with PCB 18.

Applicant respectfully submits that the arrangement wherein the heat spreader is directly attached to the bottom surface of the substrate as specified in claims 18 and 58 is neither disclosed nor remotely suggested by Selna '048. Accordingly, applicant respectfully submits that the rejection of independent claim 18, and its corresponding dependent claims 19-33, and independent claim 58 and its corresponding dependent claims 59-66, has been traversed and that, therefore, claims 19-33 and 59-66 should now be allowed.

D. Rejection of claim 21 under 35 USC §103(a)

In the *final rejection* dated October 21, 2002, the Examiner had further rejected dependent claim 21 under 35 USC §103(a) as being unpatentable over Selna' 048. As discussed above, independent claim 1 is patentably distinguishable over Selna '048 and, as such, claim 21 depending from independent claim 1 is, *a fortiori*, also patentably distinguishable over Selna '048.

**E. Rejection of claims 18-33 and 58-66 under the Judicially Created
 Doctrine of Obviousness-type Double Patenting**

In the *final rejection* dated October 21, 2002, the Examiner had provisionally rejected claims 18-33 and 58-66 under the judicially created doctrine of double patenting as being unpatentable over claims 1-20 of co-pending Application No. 09/930,747.

Along with the amendment filed on February 17, 2003 in response to the *final rejection* of October 21, 2002, Applicant had submitted a terminal disclaimer to overcome the Examiner's rejection under the judicially created doctrine of double patenting with respect to claims 1-20 of co-pending Application No. 09/930,747. Applicant respectfully submits that the filed terminal disclaimer overcomes the Examiner's double patenting rejection.

The Examiner has further rejected claims 18-33 and 58-66 under the judicially created doctrine of double patenting as being unpatentable over claims 1-17 of U.S. Patent No. 6,191,477.

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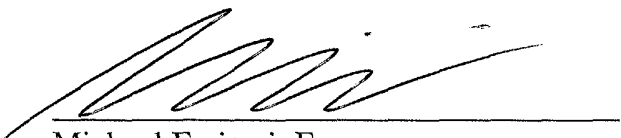
respectfully submits that the filed terminal disclaimer overcomes the Examiner's double patenting rejection.

F. Conclusion

For all the foregoing reasons, allowance of claims 18-33 and 58-66 pending in the present RCE application is respectfully requested.

Respectfully Submitted;
FARJAMI & FARJAMI LLP

Dated: 4/22/03

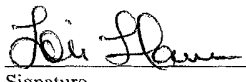

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Lori Llave
Name


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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

Claims 18 and 58 have been amended as follows:

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TC 2800 MAIL ROOM

18. (Twice Amended) A structure comprising:

a substrate having a top surface for receiving a chip;

a printed circuit board attached to a bottom surface of said substrate;

at least one signal via in said substrate;

said at least one signal via providing an electrical connection between a device electrode of said chip and said printed circuit board;

a plurality of separate thermally conductive vias in said substrate, each of said plurality of separate thermally conductive vias being coupled to a heat spreader, said heat spreader being directly attached to said bottom surface of said substrate.

58. (Twice Amended) A structure comprising:

a substrate having a top surface and a bottom surface;

a semiconductor chip attached to said top surface of said substrate;

a heat spreader directly attached to said bottom surface of said substrate;

a first plurality of separate thermally conductive vias in said substrate;

said first plurality of separate thermally conductive vias providing a connection between said semiconductor chip and said heat spreader.